

## 8.2

1

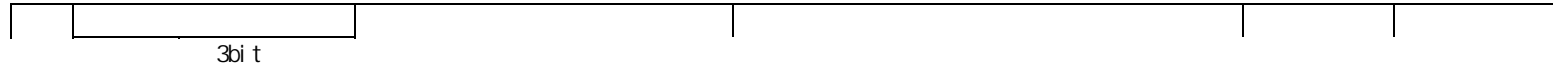
		[            ]
		DC105V
		AC152V
	CW	CW
	CCW	CCW

2

" DB"

" SB"

53H DB



		3bit						
		Bit7	Bit6	Bit5				
	84	1	0	0			DB	
	85							
	A0	1	0	1	0		DB	
	A2				2		DB	
	A3				3		DB	
	A4				4	EEPROM	DB	
	AA				10		DB	
	AC				12		DB	
	AD				13		DB	
	AE				14		DB	
	AF				15		DB	

	3bit							
	Bit7	Bit6	Bit5					
C1	1	1	0		120%		DB	
C2								
C3					4			DB
C5								DB
D1								DB
D2							1	SB
D3							2	SB
DF							5	DB
E1	1	1	1	EEPROM	EEPROM		DB	
E2				EEPROM	EEPROM			
E3				1	CPU RAM			
E4				2	CPU FIASH			
E5				1				
E6				2				
E7								
E8				CPU	CPU ASI C			
E9								
EE				1				
EF				2				
F1					CPU			DB
F2								

1)

2)

S-RDY

1.5 2

PFDDLY GroupB ID16

3)

4)

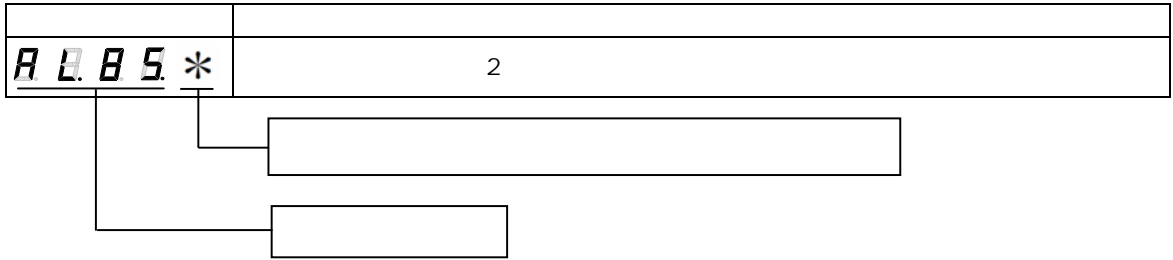
ON

5)

1s

8.3

1



0		(P-CFF)
2		(P-CN)
4		(S-RDY)
8	ON	(S-CN)
9		(CSETRDY)
A		(EMR)
F		

2

21 ( )



		1	2	3	4
ON					

1	U V W U V W	
2	U V W	
3		
4		55

22 ( 0)

	1	2
ON		

☀☀☀☀☀  
AL22\*

1		
2		

23 ( 1)

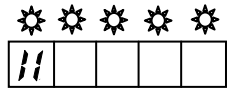
24 ( 2)

	1	2

☀☀☀☀☀  
AL23\*

☀☀☀☀☀  
AL24\*

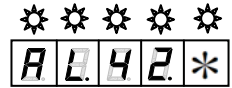
1		
2		



41 ( 1)

	1	2	3	4	5	6	7
ON							

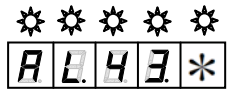
1		
2		TRMS
3		
4		
5	U V W	
6	U V W	
7		



42 ( )

	1	2	3	4	5	6	7
ON							

1		
2	50m n- 1 2	(TCM) 2 2
3		
4		
5	U V W	
6	U V W	
7		



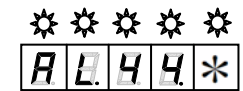
43 ( )

	1	2	3	4	5	6	7	8

1		
2		
3		
4		
5		
6		
7		
8	I D02 (02)	" "

I D02

44

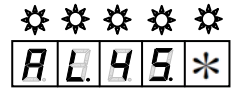


	1	2

1	
2	

45

	1



1	

51 ( )

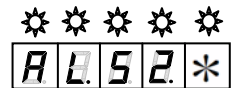
	1	2	3	4



1	
2	
3	55
4	

52 ( )

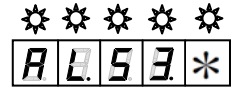
	1	2	3



1	
2	
3	55

53 ( )

	1	2	



1			
2			

55 ( )

	1	2	

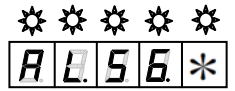


1		Group9   D40 00 _Al vays_Di sabl e	
2			

	1	2	3		

1			
2			
3			

56 ( )



	1	2	3	4
CV				

1	U V W U V W	
2	U V W	
3		
4		55

61 ( )

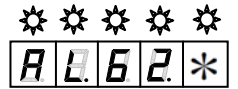


	1	2	3	4

1		
2		
3		
4		

62 ( )

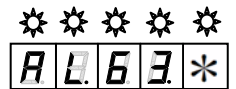
					1	2	3	4	5



1			
2			
3			
4	R S T	OFF	
5		R S T	

63 ( )

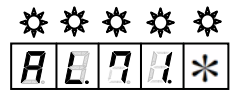
			1	2	3



1	R S T		
2			
3		I DO1	[ ]

71 ( )

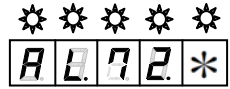
			1	2	3



1			
2			
3			

72 ( 1)

		1	2



1			
2			

73 ( 2)

		1	2



1			
2			

84 ( )

		1	2	3

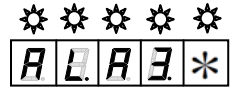


1			
2			
3			



A3 ( 3)

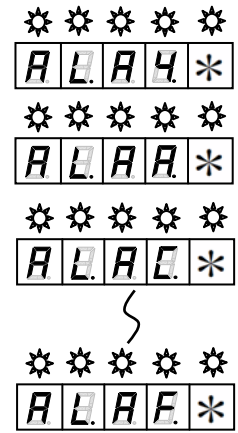
		1	2	3



1			
2			
3			

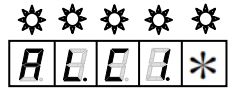
A4 ( 4)  
 AA ( 10)  
 AC AF ( 12 15)

		1	2



1			
2			

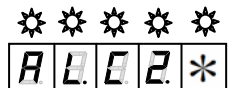
C1 ( )



	1	2	3	4
Q1				

1		
2		
3		
4	U V W	

C2 ( )




	1	2	3
Q1			

	U V W	
1		
2	( )	( )
3		

C3 ( )

	1	2	3

  
**A L C E \***

1		
2		
3	( )	( )

C5 ( )

	1	2	3

  
**A L C E \***

1		
2		
3		

D1 ( )

	1	2	3	4	5	6	7	8	9	10	11	12
	Q1											

D3 ( ) 2)

		1	2



1			
2			

DF ( )

		1



1		( )	

E1 (EEPROM )

		1



1			

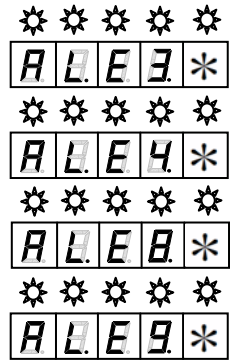
E2 (EEPROM )

		1	2



1	CPU	EEPROM	
2	EEPROM		

E3 ( 1)  
 E4 ( 2)  
 E8 (CPU )  
 E9 ( )



	1

1	

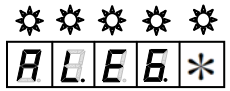
E5 ( 1)



	1	2

1	
2	

E6 ( 2)

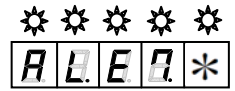


	1	2

1	
2	

E7 ( )

		1	2



1	CPU	EEPROM	
2	EEPROM		

EE ( ) 1)

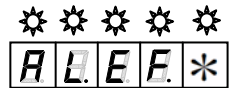
		1



1			

EF ( ) 2)

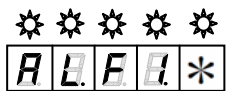
		1	2



1			
2			

F1 ( )

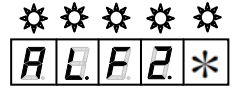
		1



1			

F2 (            )

	1	2



1		
2		